before the capacitor 64 begins charging through the pass gate transistor 62.

After the supply voltage has reached its designated output level for the desired time period, the output 47a is high and the output 47b is low in one embodiment. These signals are conveyed to the hysteresis sense stages 48a and 48b. The output of the hysteresis sense stage 48a may be coupled to a logic functionality 52.

The logic functionality 52 determines whether the signal is at an appropriate level to accurately trigger the logic in the functional blocks being initialized. While a variety of different techniques may be utilized for testing the output of one or more hysteresis sense stages 48, in one embodiment, the most difficult logic to trigger may be emulated in the logic functionality 52. In some embodiments, the toughest logic is an inverter-like stage with stacked p-channel transistors because such a stage has particularly poor headroom.

If the power supply voltage level is too low, the decision logic 54 yields a pulse that may be applied as indicated in Figure 1 for example. The decision logic 54 receives signals from the hysteresis sense stages 48a and 48b. The decision logic 54 generates a high pulse if the ground connected capacitor 64 did not charge up to Vcc or the power connected capacitor 56 did not charge up to Vss or the functional logic 52 did not pass the signal. The

pulse generator 16 continues during the power supply ramp up. When that ramp up is over for a sufficient period of time, the decision logic 54 causes the pulse generator 16 output to go away.

Figures 7 and 8 show activation circuits 40 in accordance with one embodiment. The activation circuit 40a receives the feedback signal 55a. In the case where the output pulse is low, meaning that the pulse generator 16 pulse has gone away because the desired power supply conditions have been meet, the inverter 64a inverts the low input signal 55a to a high output on the gate of the N-channel transistor 66a. This enables the transistor 66a to conduct. If the supply voltage (Vcc) is sufficient, the transistors 66a and 70a conduct.

Thus, the activation circuit 40a, in one embodiment, is not triggered until the supply voltage has reached a level sufficient to activate both transistors 66a and 70a. At this point the supply voltage should have reached a voltage level greater than two N-channel transistor threshold voltages or in one embodiment approximately 1.4 volts.

When the activation circuit 40a turns on, it shorts the capacitor node 53a in the ensuing capacitor circuit 44. In particular, the node 53a is pulled harder towards ground. This pulls the output 47b harder towards ground and tends to latch the pulse generator 16 in its deactived

state. In one embodiment, the transistor 70a may be stronger than the transistor 58.

Likewise, the circuit 40b, shown in Figure 8, receives the low input 55b and provides it to the gate of a P-channel transistor 66b. The P-channel transistor 66b turns on and turns on the transistor 70b when the threshold voltages of the transistors 66b and 70b are exceeded. When this happens, the transistor 70b decouples the capacitor 64 from the rest of the circuit and effectively latches a high output 47a through the node 53b.

Thus, the circuits shown in Figures 7 and 8 tend to latch the capacitor circuits 44 (shown in Figure 6) into their deactivated states (indicating that the output pulse is no longer needed). In particular, the circuits 40 make it harder to retrigger the pulse generator 16 prior to a power cycle.

Latching the critical nodes 53 from one threshold voltage above Vss to Vss may increase noise immunity in some embodiments. This may be useful, for example, for noise protection in low voltage applications, such as .7 volt applications. When the supply capacitor 56 is connected through a diode connected transistor 58 to ground, noise on the voltage supply (Vcc) can cause the diode node 53a to bounce. This bouncing can trigger a stage 48. The likelihood of this occurring may be reduced by using the latching operation in one embodiment.